

**Advanced Digital System Design**

**ECE 594-Online Offering-Spring 2018**

**Assignment4- Due date: March 27**

A DMA (direct memory access) output interface (DOI) for a device with an output buffer of 256 words (16 bits) is to be designed. The processing element (which is of no concern of this problem) keeps writing 16-bit data into the buffer memory. When the buffer is full, the full flag becomes 1, and the output interface (DOI) starts transmitting data to an external memory. The processing element also provides a 16-bit starting address for the data to be written into the memory, which becomes available to the DOI as a 16-bit input. All system busses are 16 bits. The entire buffer must be written into the memory, and when done, the done output of the output interface becomes 1. Only at this time the processing element can write into the buffer again. Data written into the memory should be in bursts of four words, thus the entire buffer will be written into the memory in 64 separate bursts. To obtain the bus, the output interface circuit issues a request signal (req) and waits for grant (gnt). When bus is granted it transfers four words to the memory. Writing into the memory is done by asserting chip-select (cs) and issuing nemWrite. When writing is complete, memReady becomes 1 for a clock period and return to 0.

A) Show the complete datapath of DOI, including the components and necessary internal signals.

B) Draw a state diagram that shows the behavior of your controller and issuance of control signals. Include all input and output control signals.

C) Show wiring between the datapath and the controller.

D) Write VHDL code for the design.

E) Write a comprehensive testbench and verify the circuit of Part D.